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PATENT
Attorney Docket No.: 053785-5045

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
Byeong-Dae CHOI	)	Confirmation No. 5637
Application No.: 10/032,056	)	Group Art Unit: 2815
Filed: December 31, 2001	)	Examiner: M. Warren
For: ARRAY SUBSTRATE FOR A LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME	)	**Mail Stop Appeal Brief - Patents**

Commissioner for Patents
U.S. Patent and Trademark Office
Mail Stop Appeal Brief-Patents
Alexandria, VA 22314

APPELLANT'S BRIEF TRANSMITTAL FORM

1. Transmitted herewith is the Appellant's Brief Under 37 C.F.R. § 41.31, which is being submitted further to the Notice of Appeal filed January 30, 2006.

2. Additional papers enclosed.

- ☐ Drawings: ☐ Formal ☐ Informal (Corrections)
- ☐ Information Disclosure Statement
- ☐ Form PTO-1449, ___ references included
- ☐ Citations
- ☐ Declaration of Biological Deposit
- ☐ Submission of "Sequence Listing", computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.

3. Oral Hearing Under 37 C.F.R. 1.194

☐ Oral hearing is hereby requested.
☐ Fee under 37 C.F.R. 1.17(d) is enclosed.

4. Extension of time

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ Appellant petitions for an extension of time, the fees for which are set out in 37 CFR 1.17(a)-(d), for the total number of months checked below:

Total months requested	Fee for extension	[fee for Small Entity]
☐ one month	$ 120.00	$ 60.00
☐ two months	$ 450.00	$ 225.00
☐ three months	$ 1,020.00	$ 510.00
☐ four months	$1,590.00	$ 795.00
☐ five months	$2,160.00	$1,080.00

Extension of time fee due with this request: **$ 0.00**

If an additional extension of time is required, please consider this a Petition therefor.

5. Fee Payment

☐ No fee is to be paid at this time.

☒ The Commissioner is hereby authorized to charge **$500.00** for the Appellant's Brief filing fee due to Deposit Account No. 50-0310.

☒ The Commissioner is hereby authorized to charge any fees including fees due under 37 CFR 1.16 and 1.17 which may be required, or credit any overpayment to Deposit Account No. 50-0310.

Respectfully submitted,

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Date: March 22, 2005

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APPELLANT'S BRIEF UNDER 37 C.F.R. § 41.31

This brief is in furtherance of the Notice of Appeal, filed in the above-identified patent application on January 30, 2006. The fee set forth under 37 C.F.R. § 41.20(b)(2) is being filed concurrently herewith.

1. The Real Party In Interest

The real party in interest in this appeal is LG.Philips LCD Co, Ltd. of Seoul, Korea.

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2. Related Appeals and Interferences

Appellant is not aware of any other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the appeal.

3. Status of Claims

The status of the claims is as follows:

Claims rejected: 1-14.
Claims objected to: none.
Claims allowed: none.
Claims withdrawn: 16-29.
Claims canceled: 15.
Claims appealed: 1-14.

4. Status of Amendments

No Amendments have been filed subsequent to the Final Office Action dated August 31, 2005. Accordingly, pending claims are attached as Appendix A to this brief.

5. Summary of the Claimed Subject Matter

An aspect of Appellant's present invention relates generally to an array substrate for a liquid crystal display device implementing transparent pixel electrodes, data lines, and source and drain electrodes.

Independent Claim 1

With respect to independent claim 1, as discussed in Appellant's specification beginning at paragraph [0033] at page 12 and shown in FIGs. 4-6, an array substrate for a liquid crystal display device includes a substrate 111, a plurality of gate lines 125 arranged transversely on the substrate 111, a plurality of data lines 127 disposed orthogonal to the plurality of gate lines 125, a plurality of thin film transistors T formed on the substrate 111 adjacent to intersections of the gate lines 125 and the data lines 127, each thin film transistor T including

a gate electrode 132 , a gate insulation layer 141, an active layer 145a, an ohmic contact layer 145b, a source electrode 133, and a drain electrode 135, a plurality of pixel electrodes 117 disposed at pixel regions P defined by the intersections of the gate lines 125 and the data lines 127, each pixel electrode 117 connected to a corresponding one of the drain electrodes 135, and a metal layer 128 formed on an entire surface of each of the data lines 127 and at peripheral portions of the drain electrode 135, wherein the drain electrode 135 and the pixel electrodes 117 are formed from the same material.

6. Grounds of Rejection To Be Reviewed On Appeal

Claims 1-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Related Art FIGs. 2 and 3F in view of Kakuda et al. (US 5,162,933).

7. Argument

(i) Rejections under 35 U.S.C. § 112, first paragraph

No claims are presently rejected under 35 U.S.C. § 112, first paragraph.

(ii) Rejections under 35 U.S.C. § 112, second paragraph

No claims are presently rejected under 35 U.S.C. § 112, second paragraph.

(iii) Rejections under 35 U.S.C. § 102

No claims are presently rejected under 35 U.S.C. § 102.

(iv) Rejections under 35 U.S.C. § 103

Claims 1-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's Related Art FIGs. 2 and 3F in view of Kakuda et al. (US 5,162,933). Appellant respectfully traverses the rejection as being based upon Appellant's Related Art and a reference that neither teach nor suggest the novel combination of features recited by independent claim 1, and hence dependent claims 2-14.

The Office Action admits that Appellant's Related Art FIGs. 2 and 3F discloses all the features of claim 1, "except the metal layer formed on an entire surface of each of the data lines." Accordingly, the Office Action relies upon Kakuda et al. for allegedly showing "an LCD device having a data line 11b with a metal layer formed on the entire surface." In addition, the Office Action alleges that "[w]ith such a configuration, the materials of the data line provide a light blocking function, have good heat resistance, may lower the electrical resistance, and help simplify the manufacturing process because the data line can be formed simultaneously with the pixel electrode (col. 6, line 61 – col. 7, line 29)." Thus, the Office Action concludes that it would have been obvious to "modify the data line of the APAF by forming a metal layer on the entire data line as taught by Kakuda to provide a light blocking data line having good heat resistance, a specified electrical resistance, and a reduced manufacturing steps." Appellant respectfully disagrees.

Appellant respectfully asserts that Kakuda et al. is completely silent with regard to teaching that covering the ITO layer 11a with a molybdenum-base alloy layer 11b results in providing "a light blocking data line having good heat resistance, a specified electrical resistance, and a reduced manufacturing steps," as alleged by the Office Action. Moreover, Appellant respectfully asserts that the passage cited by the Office Action in Kakuda et al. is

wholly unrelated to covering the ITO layer 11a with a molybdenum-base alloy layer 11b. Furthermore, in contrast to allegation made by the Office Action, Appellant respectfully asserts that Kakuda et al. fails to teach or suggest "the materials of the data line provide a light blocking function, have good heat resistance, may lower the electrical resistance, and help simplify the manufacturing process because the data line can be formed simultaneously with the pixel electrode (col. 6, line 61 – col. 7, line 29)."

First, Appellant respectfully asserts that Kakuda et al. actually teaches (col. 6, line 62-66) that the active matrix structure according to the disclosed invention of Kakuda et al. "permits a substantial reduction of the leakage currents which result from the irradiation of the thin film transistors by light and allows a substantial increase in the amount of charge which can be stored in the pixel capacitances." Specifically, Appellant respectfully asserts that Kakuda et al. actually is referring to the benefits of the light blocking layer and storage capacitance electrode (col. 6, lines 4-12), wherein:

> [w]ith the active matrix structure described above, it is possible to effectively prevent deterioration of the display image quality, partly because the provision of the light blocking layer 18 affords substantial reduction of the leakage current which is caused by the incidence of light to the thin film transistor 20, and partly because the provision of the storage capacitance electrode 17 allows a substantial increase in the amount of charge to be stored in the pixel electrode 14.

Thus, Appellant respectfully asserts that the alleged motivation provided by the Final Office Action, i.e., "the materials of the data line provide a light blocking function, have good heat resistance, may lower the electrical resistance," is clearly not directed toward any structure associated with the data line structure 11 disclosed by Kakuda et al. As discussed above, the motivation alleged by the Final Office Action to be taught by Kakuda et al. is clearly directed

toward benefits of the light blocking layer and the storage capacitance electrode, and not to any data line structure disclosed by Kakuda et al.

Appellant respectfully asserts that a fair reading of the entire Specification illustrates that the disclosure of Kakuda et al. (col. 6, line 61 – col. 7, line 29) relied upon by the Final Office Action is clearly directed toward benefits obtained from the light blocking layer, the storage capacitance electrode, and the storage capacitance lines. Specifically, Appellant respectfully asserts that Kakuda et al. explicitly discloses (col. 6, lines 12-17) that:

> [f]urthermore, since the light blocking layers 18, the storage capacitance electrodes 17 and the storage capacitance lines 29 are formed by the same layer of the same material, the number of manufacturing steps is minimized, and consequently, the manufacturing costs are low.

Thus, Appellant respectfully asserts that the alleged motivation provided by the Final Office Action, i.e., "[w]ith such a configuration...help simplify the manufacturing process because the data line can be formed simultaneously with the pixel electrode," is clearly not directed toward any structure associated with the data line structure 11 disclosed by Kakuda et al. In fact, the motivation alleged by the Final Office Action to be taught by Kakuda et al. is clearly directed toward benefits of the light blocking layer, the storage capacitance electrode, and the storage capacitance lines, and not to any data line structure disclosed by Kakuda et al.

Accordingly, Appellant respectfully asserts that the alleged motivation cited in the Final Office Action is wholly unrelated to features of the data lines of Kakuda et al. In other words, although Kakuda et al. may disclose benefits (col. 6, line 61 to col. 7, line 29) associated with an active matrix structure for a liquid crystal display device, Kakuda et al. is completely silent with regard to providing any motivation, either implicitly or explicitly, with

which to modify the data line structure shown in Appellant's Related Art FIGs. 1-3 in order to arrive at Appellant's claimed invention. Accordingly, Appellant respectfully asserts that the Final Office Action fails to establish a *prima facie* case of obviousness with regard to at least independent claim 1, and hence dependent claims 2-14, since the Final Office Action fails to cite any proper motivation with which to modify any of Appellant's Related Art FIGs. 1-3.

MPEP 2143.01 instructs that "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)." Accordingly, since Kakuda et al. fails to provide any proper motivation with which to modify any of Appellant's Related Art FIGs. 1-3, or suggest the desirability of combining the teachings of Kakuda et al. with any of Appellant's Related Art FIGs. 1-3, then the resultant combination is not obvious.

With regard to the Response to Arguments section of the Final Office Action, Appellant respectfully asserts that the comments set forth therein fail to successfully rebut Appellant's arguments regarding establishment of a *prima facie* case of obviousness with regard to at least independent claim 1, and hence dependent claims 2-14. Specifically, Appellant respectfully asserts that the disclosure relied upon by the Final Office Action fails to provide any proper motivation with which to modify any of Appellant's Related Art FIGs. 1-3.

First, the rebuttal offered by the Final Office Action that "[a]s stated in the rejection above, column 6, line 61 – column 7, line 29 disclose the motivation for forming the metal layer on the surface of the data lines" is clearly not supported by the disclosure of Kakuda et

al. for at least Appellant's reasons set forth above. Accordingly, the rebuttal provided by the Final Office Action fails to successfully rebut Appellant's arguments that Kakuda et al. fails to provide proper motivation with which to modify any of Appellant's Related Art FIGs. 1-3.

Second, the rebuttal offered by the Final Office Action that "[i]n column, 7 lines 8-29, Kakuda discloses the specific benefits of using metal materials such as aluminum or molybdenum as part of the data lines, gate lines, light blocking layers, etc." is incorrect. Although Kakuda et al. discloses (col. 7, lines 13-15) that "[a]luminum is particularly suited for the lines 11, 13 and 29 because it is low in electric resistance," Kakuda et al. continues to explicitly disclose (col. 7, line 66 to col. 8, line 5) the disadvantages of using an aluminum-molybdenum laminated films, i.e., formation of overhangs and differing etch rates. Thus, Kakuda et al. explicitly teaches away from Appellants' claimed invention. Accordingly, the rebuttal provided by the Final Office Action fails to successfully rebut Appellant's arguments that Kakuda et al. fails to provide proper motivation with which to modify any of Appellant's Related Art FIGs. 1-3.

Third, the rebuttal offered by the Final Office Action that "[a]pparently, molybdenum is suitable as a wiring material because of its heat resistance and its workability by chemical etching" fails to establish any proper motivation to modify any of Appellant's Related Art FIGs. 1-3. Specifically, Appellant respectfully asserts that Kakuda et al. explicitly discloses (col. 7, lines 20-22) that molybdenum is "appreciably higher in its electric resistance than aluminum (Al)." Although Kakuda et al. may disclose that molybdenum is widely employed as a material for electrodes, Kakuda et al. also discloses (col. 7, lines 35-43) that both open-circuit and short-circuit conditions are caused by its use as a material with which to form conductive lines. In fact, Kakuda et al. lists a number of disadvantages of using molybdenum

as a material with which to form conductive lines. Accordingly, the statement provided by the Final Office Action fails to successfully rebut Appellant's arguments that Kakuda et al. fails to provide proper motivation with which to modify any of Appellant's Related Art FIGs. 1-3.

Fourth, the rebuttal offered by the Final Office Action that "[i]n column, 7, lines 44-67, Kakuda discloses the known practice of forming laminated matrix lines of ITO and metal in an active matrix LCD device to reduce the resistance of lines" is completely taken out of context with regard to the entire disclosure of Kakuda et al. Specifically, Appellant respectfully asserts that Kakuda et al. explicitly discloses that:

> ...in an active matrix LCD (liquid crystal display), it is desirable, for the purpose of reducing the resistance of matrix lines, to employ a laminated structure in which an aluminum film overlies the ITO film forming the transparent electrode, *but direct lamination of the ITO and aluminum (Al) films poses a problem as the ITO is corroded by preferential dissolution resulting from galvanic action between the dissimilar metals.*

Furthermore, Kakuda et al. discloses (col. 7, lines 51-59) the different failures associated with using aluminum-molybdenum laminated films. Accordingly, Appellant respectfully asserts that Kakuda et al. actually discloses the disadvantages of using the known practice of forming laminated conductive lines in LCD devices. Thus, the rebuttal provided by the Final Office Action fails to successfully rebut Appellant's arguments that Kakuda et al. fails to provide proper motivation with which to modify any of Appellant's Related Art FIGs. 1-3.

Fifth, the rebuttal offered by the Final Office Action that "[a]lthough col. 6, line 61 – col. 7, line 7 specifically discloses the invention's benefits as they pertain to the active matrix as a whole, the benefits still pertain to the data line portion as well because the data line is a

part of the LCD active matrix" is incorrect. Appellant respectfully asserts that the explicit disclosure of Kakuda et al. at col. 6, line 61 to col. 7, line 7 specifically points out the disadvantages of using aluminum-molybdenum laminated conductive lines in AM-LCD devices. As such, the Final Office Action's conclusion that "benefits" disclosed by Kakuda et al. (col. 6, line 61 to col. 7, line 7) are, at best, contradictory to the explicit disclosure of Kakuda et al. For example, the Final Office Action maintains that "benefits" are disclosed by Kakuda et al. at col. 6, line 61 to col. 7, line 7, but the actually language of Kakuda et al. is all directed toward the negative results from using laminated films for AM-LCD device. Thus, the rebuttal provided by the Final Office Action fails to successfully rebut Appellant's arguments that Kakuda et al. fails to provide proper motivation with which to modify any of Appellant's Related Art FIGs. 1-3.

Sixth, the rebuttal offered by the Final Office Action that "[t]he lines that have been recited in this argument show specific benefits for the use of a metal layer on the data lines and this shows proper motivation for combining with the APAF" is completely unsupported by the cited portions of Kakuda et al. of the reasoning set forth in the Final Office Action. Appellant respectfully asserts that the Final Office Action has failed to cite any portions of Kakuda et al. that properly provide any motivation whatsoever with which to combine the teachings of Kakuda et al. and any of Appellant's Related Art FIGs. 1-3. In fact, the Final Office Action repeatedly attempts to redefine the disclosure (col. 6, line 61 to col. 7, line 29) of Kakuda et al. as explaining the "benefits" of using a laminated conductive line structure, whereas Kakuda et al. continuously discloses the disadvantages of using a laminated conductive line structure, i.e., breakage of wires and shorting of the wires. Thus, the rebuttal provided by the Final Office Action fails to successfully rebut Appellant's arguments that

Kakuda et al. fails to provide proper motivation with which to modify any of Appellant's Related Art FIGs. 1-3.

For at least the above reasons, Appellant respectfully submits that claims 1-14 are neither taught nor suggested by Appellant's Related Art FIGs. 2 and 3F and Kakuda et al., whether taken alone or in combination. Thus, Appellant respectfully asserts that the rejection under 35 U.S.C. § 103(a) should be withdrawn because the above-discussed novel combination of features are neither taught nor suggested by Appellant's Related Art FIGs. and the applied reference.

(v) Other Rejections

No claims are presently rejected under grounds other than those referred to above.

* * * * *

In view of the foregoing, Appellant respectfully requests the reversal of the Examiner's rejection and allowance of the pending claims. If there are any other fees due in connection with the filing of this Appeal Brief, please charge the fees to our Deposit Account No. 50-0310.

If a fee is required for an extension of time under 37 C.F.R. §1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account No. 50-0310.

Respectfully submitted,

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8. Claims Appendix

Claim 1 (Previously Presented): An array substrate for a liquid crystal display device, comprising:

a substrate;

a plurality of gate lines arranged transversely on the substrate;

a plurality of data lines disposed orthogonal to the plurality of gate lines;

a plurality of thin film transistors formed on the substrate adjacent to intersections of the gate lines and the data lines, each thin film transistor including a gate electrode, a gate insulation layer, an active layer, an ohmic contact layer, a source electrode, and a drain electrode;

a plurality of pixel electrodes disposed at pixel regions defined by the intersections of the gate lines and the data lines, each pixel electrode connected to a corresponding one of the drain electrodes; and

a metal layer formed on an entire surface of each of the data lines and at peripheral portions of the drain electrode,

wherein the drain electrode and the pixel electrodes are formed from the same material.

Claim 2 (Original): The array substrate according to claim 1, wherein the gate insulation layer is disposed on the gate electrode.

Claim 3 (Original): The array substrate according to claim 1, wherein the active layer is disposed on the gate insulation layer, and the ohmic contact layer is disposed on the active layer.

Claim 4 (Original): The array substrate according to claim 1, wherein the source electrode and the drain electrode are disposed on the ohmic contact layer.

Claim 5 (Original): The array substrate according to claim 4, wherein the source electrode extends from one of the data lines.

Claim 6 (Original): The array substrate according to claim 4, wherein the drain electrode extends from one of the pixel electrodes.

Claim 7 (Original): The array substrate according to claim 4, wherein the drain electrode and source electrode include at least a transparent conductive material.

Claim 8 (Original): The array substrate according to claim 7, wherein each data line includes at least the transparent conductive material.

Claim 9 (Original): The array substrate according to claim 7, wherein each pixel electrode includes the transparent conductive material.

Claim 10 (Original): The array substrate according to claim 7, wherein the transparent conductive material is selected from a group including indium tin oxide, indium zinc oxide, zinc oxide, thin oxide and indium oxide.

Claim 11 (Original): The array substrate according to claim 1, wherein the gate insulation layer is disposed on the plurality of gate lines.

Claim 12 (Original): The array substrate according to claim 1, wherein the metal layer is selected from a group including aluminum (Al), copper (Cu), gold (Au) and silver (Ag).

Claim 13 (Original): The array substrate according to claim 12, wherein the metal layer is formed on an entire surface of the source electrode.

Claim 14 (Original): The array substrate according to claim 12, wherein the metal layer is formed at peripheral portions of the plurality of pixel electrodes.

Claim 15 (Canceled).

Claim 16 (Withdrawn): A method of fabricating an array substrate for a liquid crystal display device, comprising the steps of:

forming a first metal layer on a substrate;

forming a gate line and a gate electrode;

forming a gate insulation layer to cover the first metal layer;

forming a pure amorphous silicon layer and a doped amorphous silicon layer on the gate insulation layer;

forming an ohmic contact layer and an active layer over the gate electrode;

forming a transparent conductive material on the gate insulation layer to cover the active layer and the ohmic contact layer;

forming a photoresist layer on the transparent conductive material;

patterning the photoresist layer using a mask;

forming a data line, a pixel electrode, a source electrode and a drain electrode; and

forming a second metal layer on an entire surface of the data line.

Claim 17 (Withdrawn): The method according to claim 16, wherein the step of forming the gate line and the gate electrode includes patterning the first metal layer.

Claim 18 (Withdrawn): The method according to claim 16, wherein the step of forming the ohmic contact layer and the active layer includes patterning the doped amorphous silicon layer and the pure amorphous silicon layer.

Claim 19 (Withdrawn): The method according to claim 16, wherein the mask includes a plurality of slits and a plurality of light shielding areas.

Claim 20 (Withdrawn): The method according to claim 16, wherein the step of forming the data line, the pixel electrode, the source electrode, and the drain electrode includes patterning the transparent conductive material using a dry etching process.

Claim 21 (Withdrawn): The method according to claim 20, wherein the step of patterning the transparent conductive material includes removing a first photoresist layer formed on the data line and the source electrode while etching exposed portions of the transparent conductive material, and removing peripheral portions of a second photoresist layer formed on the drain electrode and the pixel electrode while etching the exposed portions of the transparent conductive material.

Claim 22 (Withdrawn): The method according to claim 16, further including the step of forming the second metal layer on an entire surface of the source electrode.

Claim 23 (Withdrawn): The method according to claim 16, further including the step of forming the second metal layer at peripheral portions of the pixel electrode and the drain electrode.

Claim 24 (Withdrawn): The method according to claim 16, wherein the step of patterning the photoresist layer includes aligning the mask over the photoresist layer, exposing light through a plurality of slits of the mask; and developing the photoresist layer to expose the transparent conductive material.

Claim 25 (Withdrawn): The method according to claim 16, wherein the step of forming the second metal layer includes electroplating a second metal material on the data line, electroplating the second metal material on the source electrode, electroplating the second metal material on peripheral portions of the pixel electrode, electroplating the second metal material on peripheral portions of the drain electrode, and removing the photoresist layer from the transparent conductive material.

Claim 26 (Withdrawn): The method according to claim 16, wherein the source electrode extends from one of the data lines.

Claim 27 (Withdrawn): The method according to claim 16, wherein the drain electrode extends from one of the pixel electrodes.

Claim 28 (Withdrawn): The method according to claim 16, wherein the transparent conductive material is selected from a group including indium tin oxide, indium zinc oxide, zinc oxide, thin oxide and indium oxide.

Claim 29 (Withdrawn): The method according to claim 16, wherein the second metal layer is selected from a group including aluminum(Al), copper(Cu), gold (Au) and silver (Ag).

9. Evidence Appendix

No information is appended under this section.

10. Related Proceedings Appendix

No information is appended under this section.